AFFICHEUR LCD
2 LIGNES DE 20 CARACTÈRES

Référence : 9513

04/2003/ZM

Produit importé et distribué par :

Selectronic

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Contents

1. BASIC SPECIFICATION

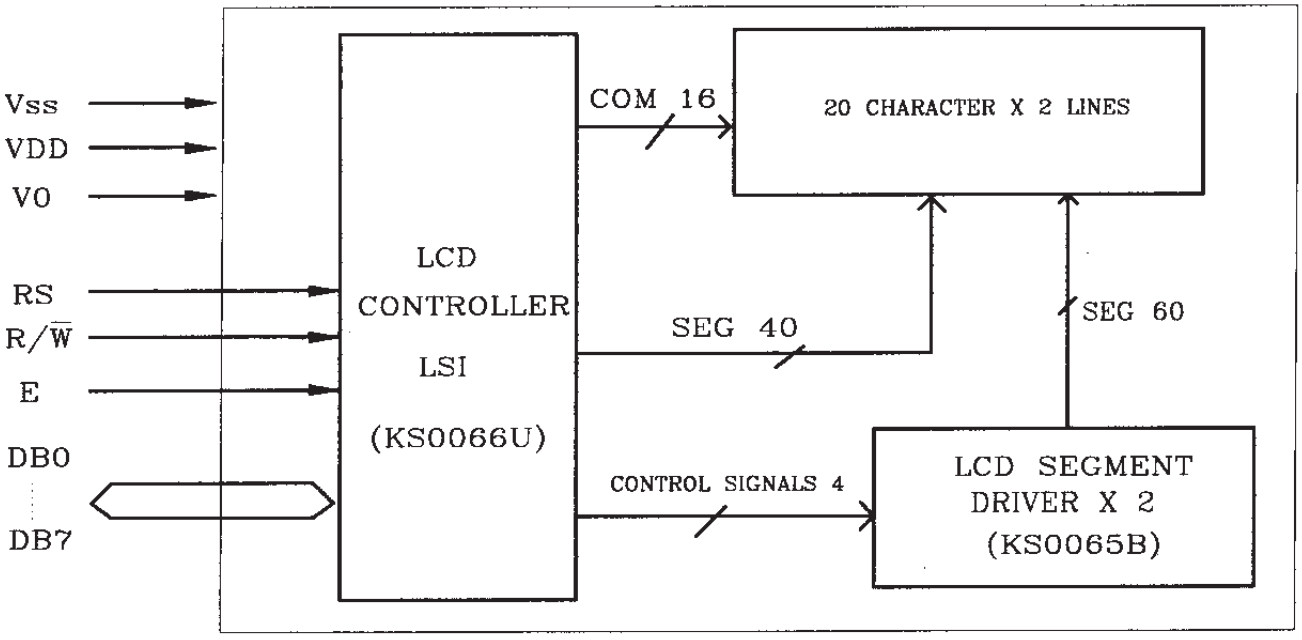
1-1 DISPLAY SPECIFICATIONS

. DISPLAY MODE : STN-TRANSFLECTIVE-POSITIVE-YELLOW-GREEN
. DISPLAY FORMAT : 20 CHARACTERS X 2 LINES
. INPUT DATA : 8-BITS PARALLEL DATA INPUT FROM A MPU
. MULTIPLEXING : 1/16 DUTY
. VIEWING DIRECTION : 6 O CLOCK
. DRIVED IC : KS0066U(1Chip) + KS0065B (2 Chips)
. BEZEL : 0.6T
. OTHERS :

1-2. MECHANICAL SPECIFICATION

ITEM	SPECIFICATIONS	UNIT	REMARK
DIMENSIONAL OUTLINE	116.0(W)×37.0(H)×9.5MAX.(T)	mm	*REFERENCE DIMENSIONAL OUTLINE
VIEW AREA	83.0(W)×18.6(H)		
EFFECTIVE V/AREA	75.4(W)×11.5(H)		
NUMBER OF CHARACTERS	20 CHARACTERSX2LINES	--	
DOT PITCH	0.65(W)×0.70(H)	mm	
DOT SIZE	0.60(W)×0.65(H)	mm	

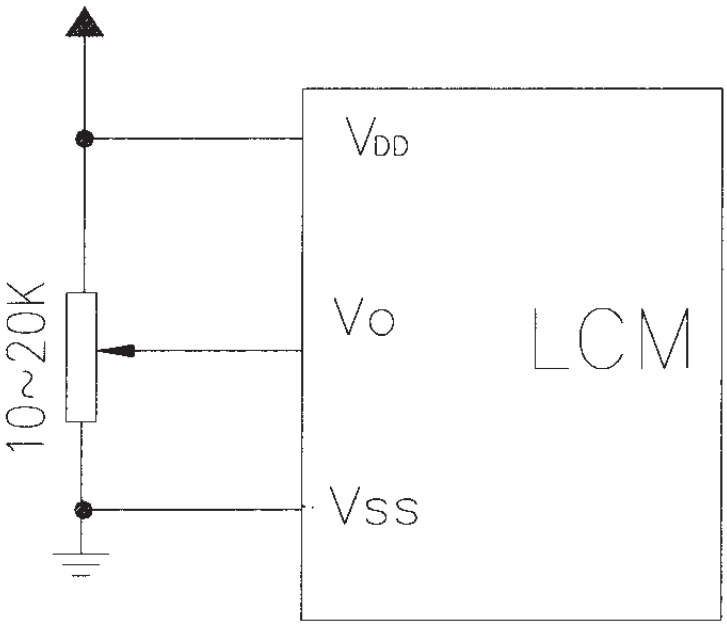
1-3 BLOCK DIAGRAM



1-4 TERMINAL FUNCTIONS

PIN NO	SYMBOL	LEVEL	DESCRIPTION
1	Vss	-	GROUND
2	VDD	-	POWER SUPPLY FOR LOGIC
3	Vo	-	POWER SUPPLY FOR LCD
4	RS	H/L	REGISTER SELECTION
5	R/W	H/L	READ/WRITE
6	E	H, H/L	ENABLE SIGNAL
7	DB0	H/L	DATA BIT0
8	DB1	H/L	DATA BIT1
9	DB2	H/L	DATA BIT2
10	DB3	H/L	DATA BIT3
11	DB4	H/L	DATA BIT4
12	DB5	H/L	DATA BIT5
13	DB6	H/L	DATA BIT6
14	DB7	H/L	DATA BIT7

1-5 POWER SUPPLY CIRCUIT AND CONTRAST ADJUST



2. ABSOLUTE MAXIMUM RATINGS (Ta=25 °C, Vss=0V)

PARAMETER	SYMBOL	RATINGS			UNITS
		MIN.	TYP.	MAX.	
POWER SUPPLY FOR LOGIC	VDD-Vss	0	-	7.0	V
POWER SUPPLY FOR LCD DRIVER	VDD V0	0	-	12.0	V
INPUT VOLTAGE	VIN	Vss	-	VDD	V
OPERATING TEMPERATURE	Topr	0	-	50	°C
STORAGE TEMPERATURE	Tstg	-20	-	70	°C

3.ELECTRICAL & OPTICAL CHARACTERISTICS

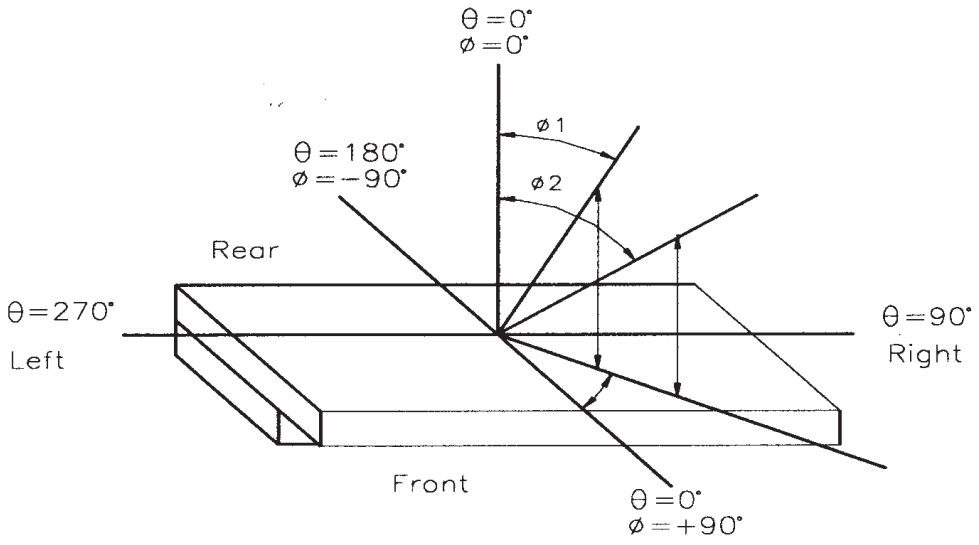
3-1 ELECTRICAL CHARACTERISTICS (Ta=25°C)

ITEM	SYMBOL	CONDITION	MIN	TYPE	MAX.	UNIT
LOGIC CIRCUIT POWER SUPPLY VOLTAGE	V_{DD}-Vss		4.5	5.0	5.5	V
INPUT VOLTAGE	V_{IH}		2.2		V_{DD}	V
INPUT VOLTAGE	V_{IL}		Vss		0.6	V
LOGIC CIRCUIT POWER SUPPLY CURRENT	I_{DD}	V_{DD}-Vss=5.0V		2.0	3.0	Ma
RECOMMENDED LCD DRIVING VOLTAGE	V_{DD}-V0 ϕ=0 θ=0	Ta=25 °C		5.0		V
FRAME FREQUNCY	f_{FLM}	-	-	128	-----	Hz

3-2. ELECTRO OPTICAL CHARACTERISTICS(Ta=25 °C V_{DD}=5.0±0.25V)

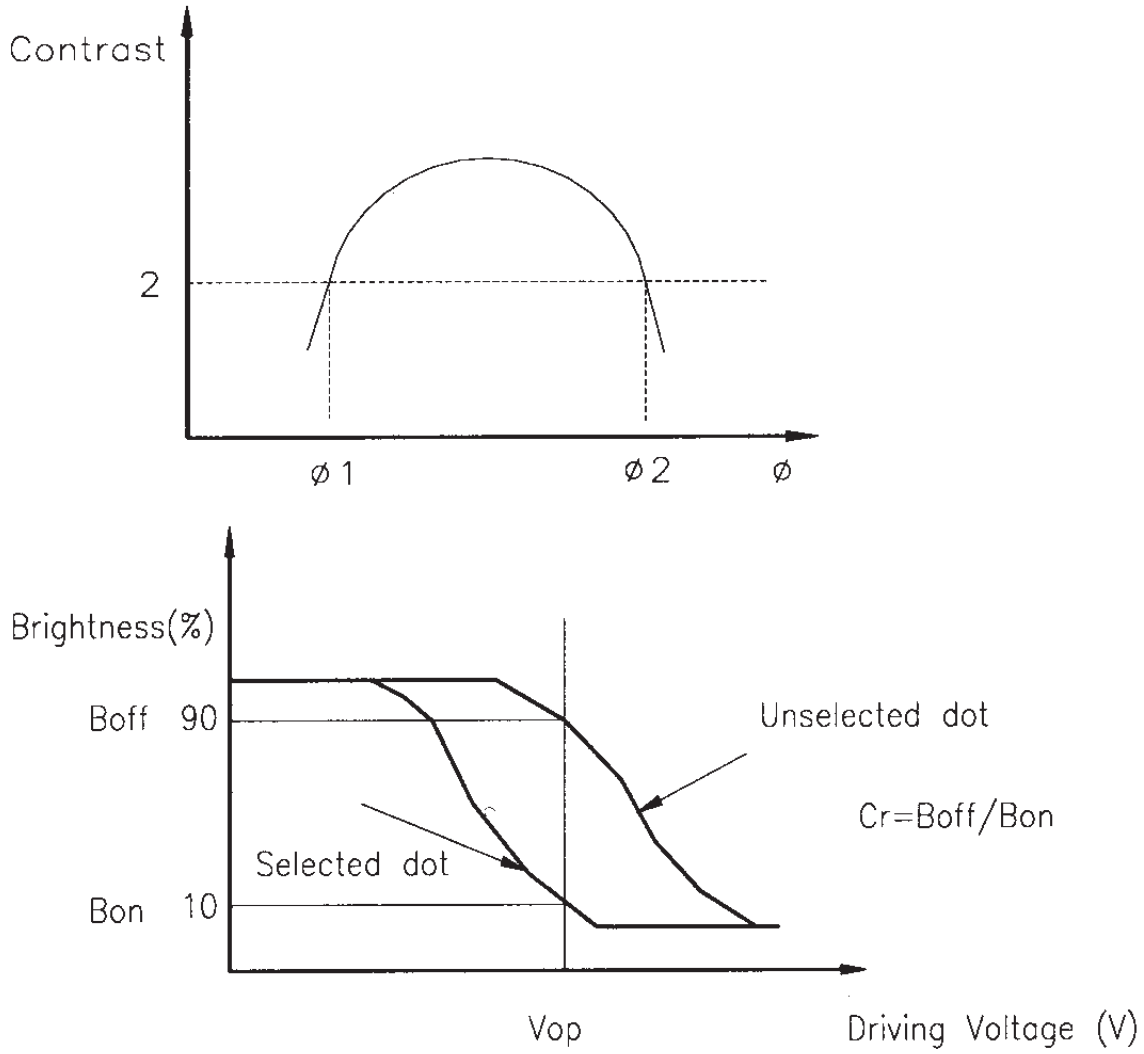
ITEM	SYMBOL	CONDITION	MIN	TYPE	MAX	UNIT
VIEW ANGLE	ϕ	θ=0°(Cr≥2) 0°<ϕ1, ϕ2<90°	35	40		Deg
CONTRAST	Cr	ϕ=15°,θ=0° 6 O'CLOCK	3	5		
RESPONSE TIME	tr(rise)	6 O'CLOCK		250	350	ms
	tf(fall)	ϕ=15°,θ=0°		250	350	ms

NOTE1: Definition of Viewing Angle θ,ϕ

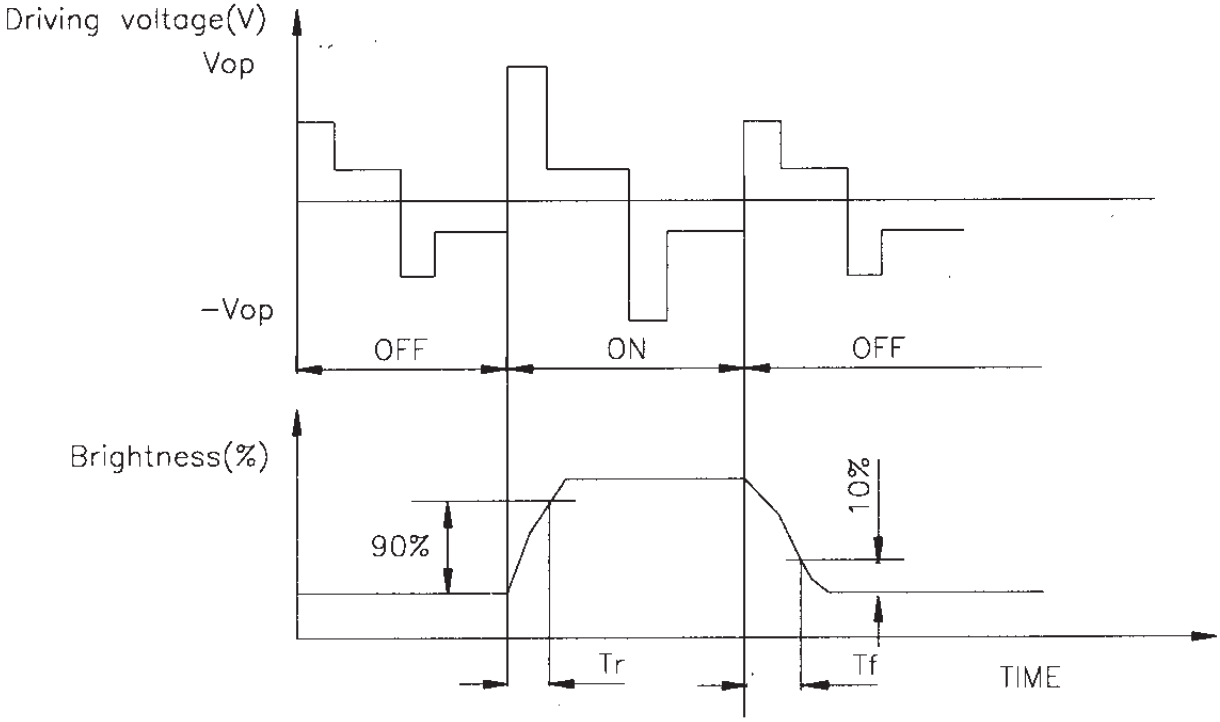


NOTE2: Definition of viewing Angle Range: ϕ=|ϕ2-ϕ1|

NOTE3: Definition of Contrast



NOTE4: Definition of Response Time



5. FUNCTION DESCRIPTION& INSTRUCTION SET

5-1. FUNCTION DESCRIPTION (KS0066U)

System Interface

This chip has both kinds of interface type with MPU: 4-bit bus and 8-bit bus.
4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bits registers are used.
One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction.
Each internal operation, reading from or writing into RAM, is done automatically.
Thus, after MPU read DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction codes transferred from MPU.
MPU cannot use it to read instruction data.

To select a register, you can use RS input pin in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction Write operation (MPU write Instruction code into IR)
L	H	Read Busy flag(DB7) and address counter (DB0 to DB6)
H	L	Data Write operation (MPU write data into DR)
H	H	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

BF= "High", indicates that the internal operation is being processed.
So during this time the next instruction cannot be accepted. BF can be read through DB7 port when RS = "Low" and R/W = "High" (Read Instruction Operation).
Before executing the next instruction, be sure that BF is not "High".

Address Counter (AC)

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS= "Low" and R/W= "High", AC can be read through ports DB0 to DB6.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80X8 bits (80 characters).
DDRAM address is set in the address counter(AC) as a hexadecimal number (Refer to Fig-1.)

MSB LSB

AC6	AC5	AC4	AC3	AC2	AC1	AC0

Figure 1. DDRAM Address

20 character * 2 line:

Line 1	Display position	1	2	3	4	.....	19	20
	DDRAM address	00H	01H	02H	03H	.....	12H	13H
Line 2	Display position	1	2	3	4	.....	19	20
	DDRAM address	40H	41H	42H	43H	.....	52H	53H

CGROM (Character Generation ROM)

CGROM has a 5x8 dots 204 characters pattern and a 5x11 dots 32 characters pattern (Refer to the CGROM Character Code Table)

CGROM has 204 characters pattern of 5x8 dots, and 32 characters pattern of 5x11 dots.

CGRAM (Character Generation RAM)

CGRAM has up to 5x8 dots 8 characters.

By writing font data to CGRAM, user defined characters can be used.

Refer to follow table.

Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)	CGRAM Address	CGRAM Data	Pattern number
D7 D6 D5 D4 D3 D2 D1 D0	A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 x 0 0 0	0 0 0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	x x x 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 0 0 0 0	pattern 1
*	* * * * * *	*	*
0 0 0 0 x 1 1 1	1 1 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	x x x 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 0 0 0 0	pattern 8

5-2. INSTRUCTION SET

5-2-1. INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between the internal clock of KS0066U and the MPU clock, KS0066U performs internal operations by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. Instructions can be divided largely into four groups:

1) KS0066U function set instructions (set display methods, set data length, etc.)
2) Address set instructions to internal RAM.
3) Data transfer instructions with internal RAM.
4) Others.

The address of the internal RAM is automatically increased by 1.

Note: During internal operation, Busy Flag (DB7) is read High .

Busy Flag check must be preceded by the next instruction.

When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the "E" signal after the Busy Flag (DB7) goes to Low .

Contents

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing 20H (space code) to all DDRAM address, and set DDRAM address to 00H into AC(address counter).

Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display.

Make the entry mode increment (I/D= High).

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	

Return home is cursor return home instruction.

Set DDRAM address to 00H into the address counter.

Return home to its original site and return display to its original status, if shifted.

Counters of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)

When I/D = High , cursor/blink moves to right and DDRAM is increased by 1.

When I/D = Low , cursor/blink moves to left and DDRAM is decreased by 1.

* CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: shift of entire display

When DDRAM read (CGRAM read/write) operation or SH = Low , shifting of entire display is not performed.

if SH = High and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = High : shift left, I/D = Low : shift RIGHT).

4 Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	D	C	B

Control display /cursor/blink ON/OFF 1 bit register.

D display on/off control bit
When D= High , entire display is turned on.
When D = Low , entire display is turned off, but display data remains in DDRAM,

C cursor on/off cursor bit
When C = High , cursor is turned on.
When C = Low , cursor is disappeared in current display, but I/D register preserves its data.

B cursor blink on/off control bit
When B = High , cursor blink is on which performs alternately between all the High data and when B = Low , blink is off.

5 Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	S/C	R/L		

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When display data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.

Shift patterns according to S/C and bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	DL	N	F		

DL: interface data length control bit
When DL= High , it means 8-bit bus mode with MPU.
When DL = Low , it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data twice.
N: display line number control mode is set.
When N= Low , 1-line display mode is set.
When N = High , 2-line display mode is set.

F: display font type control bit

When F= Low , 5 x 8 dots format display mode is set.
When F= High , 5 x 11 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N=Low), DDRAM address is from "00H" to 27H .
In 2-line display mode (N=High), DDRAM address in the 1st line is from 00H to 27H , and DDRAM address in the 2nd line is from 40H to 67H .

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066U is in internal operation or not.
If the resultant BF is High , internal operation is in progress and should wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/ decreased by 1, according to the entry mode.

11) Read Data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction if the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.
After read operation, address counter is automatically increased/ decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

Note: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.
At this time, AC indicates the next address position, but only the previous data can be read by the read instruction.

5-2-2. INSTRUCTION

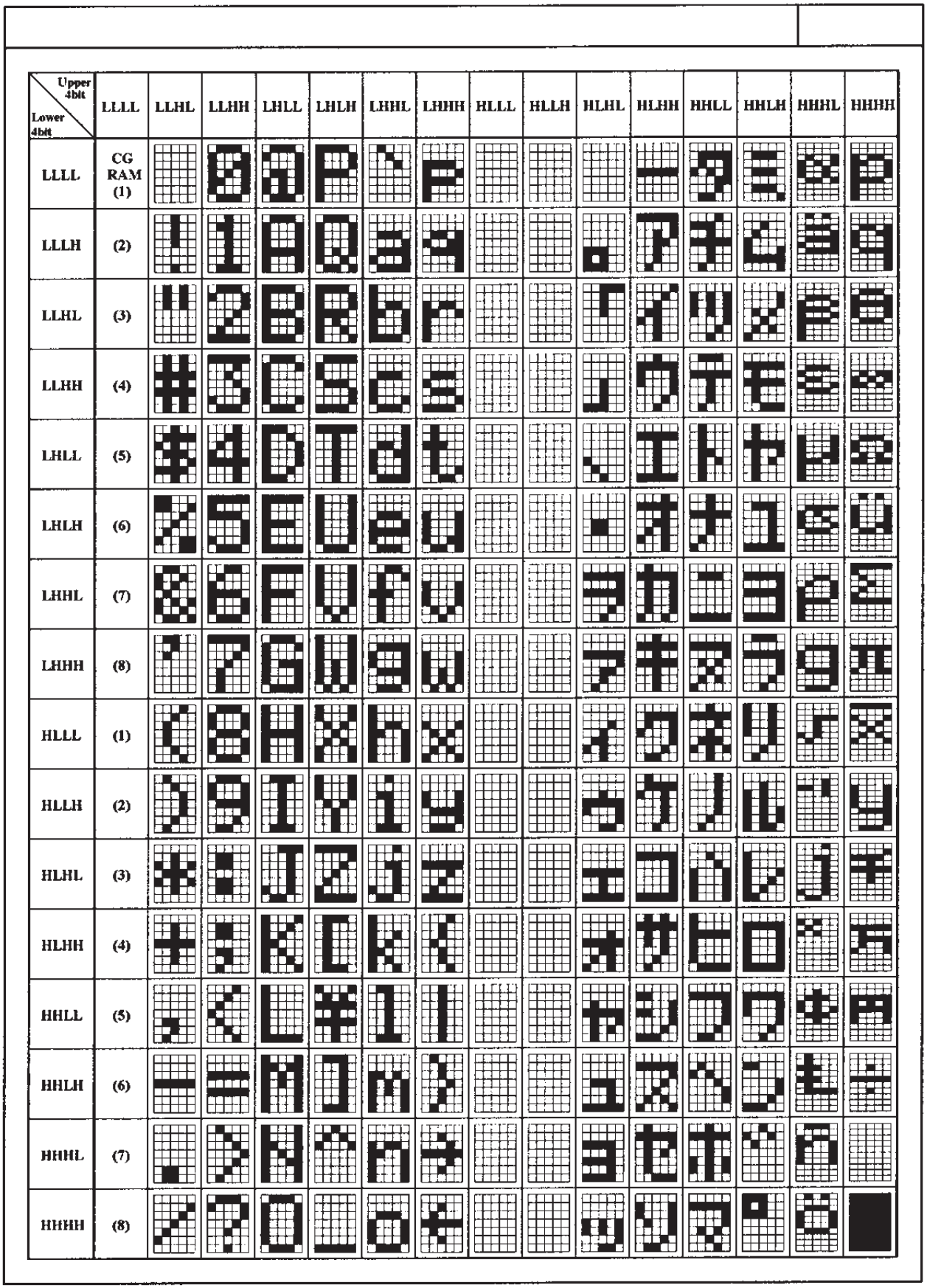
Instruction	Instruction code										Description	Execution time
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		(fosc=270KHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Write 20H to DDRAM and set DDRAM address to 00H from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to 00H From AC and return cursor to its Original position if shifted. The contents of DDRAM are not Changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And enable the shift of entire display.	39us
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39us
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F: 5x11dots/5x8dots)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address Counter.	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address Counter.	39us
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0us
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

* - : don t care

6. CHARACTER FONT TABLE

[CORRESPONDENCE BETWEEN CHARACTER CODE AND CHARACTER PATTERN]

Standard Character Pattern



7. DIMENSIONAL OUTLINE

PIN NO.	1	2	3	4	5	6	7~14
SYMBOL	Vss	Vdd	V0	RS	R/W	E	D0~D7